REMARKS

Applicants respectfully request reconsideration of the present application based on the foregoing amendments and the following remarks. Applicants herein amend the specification and claims 1, 5, 9-13 and 17. Claims 1-20 remain pending in the application.

Objections to the Specification

In the Office Action, the Examiner instructed the Applicants to remove the Appendix from the Specification. As instructed, Applicants herewith propose to amend the specification by canceling the Appendix attached as pages 36-72 to the present specification. It is assumed that the Examiner's instructions indicate that the Appendix originally filed with the specification did not affect whether the written description enabled practice of the best mode of the inventions of the originally filed claims by those skilled in the art.

Claim Rejections Under 35 U.S.C. § 112 (First Paragraph)

Claims 9, 10 and 12 stand rejected under 35 U.S.C. § 112 (first paragraph) as allegedly failing to enable the invention commensurate in scope with the claims (i.e. "undue breadth").

This rejection is respectfully traversed at least because the claims as presented were not all "single means" claims as stated in the Office Action. For example, claims 9 and 10 as presented set forth a "computer-readable storage medium" storing therein software for performing at least two distinct operations. Moreover, claim 12 originally set forth an "instruction server," and thus did not set forth every conceivable structure for performing the recited operations. Nevertheless, claims 9, 10 and 12 have been amended herewith to even further clarify the inventions that were originally claimed.

Accordingly, the rejection of claims 9, 10 and 12 under 35 U.S.C. § 112 (first paragraph) should be withdrawn.

Claim Rejections Under 35 U.S.C. § 112 (Second Paragraph)

Claim 9 stands rejected under 35 U.S.C. § 112 (second paragraph) as allegedly being indefinite. This claim has been amended as described above, and so this rejection should be

withdrawn. However, it should be clarified that the claimed software program in claim 9 is not merely directed toward "programming" a processor, but rather "generating" a configurable processor, and then debugging software to be embedded on it. As set forth in many places in the specification (for example at page 1, line 12 to page 2 line 2), the present invention is directed toward tools for observing and displaying the state of a **configurable** processor. For example, the present invention set forth in claim 9 allows a developer to debug embedded software applications running on a configurable processor that has been **generated** with custom-configured instructions and state.

Claim Rejections Under 35 U.S.C. § 102(b)

Claims 1, 2, 4-6, 8-11, 13, 14, 16-18 and 20 stand rejected under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent No. 5,896,521 to Shackleford et al. ("Schackleford"). For reasons set forth more fully below, Applicants respectfully traverse this rejection.

Amended Independent Claims 1 and 13 Patentably Define Over Shackleford

Independent claims 1 and 13 both require, *inter alia*, **transmitting** a state-accessing instruction stream from a debugger to an interpreting agent, the interpreting agent then **returning** the accessed state to the debugger.[1] These claims have been amended herewith for formality purposes not related to patentability.

As set forth in the specification at, for example, page 2, line 3 to page 8, line 2, the present invention relates to providing embedded software development capabilities for configurable processors. One desired capability for debugging or evaluating embedded software to be run on a configurable processor is to access the state of the processor. The prior art approaches to accessing state have many problems. Accordingly, as set forth in the specification at, for example, page 10, lines 3-9, the present invention includes, for example, two aspects: a software system including a debugger that is capable of transmitting instruction sequences for processor state access to a state-access mechanism in the processor; and a state access mechanism that is capable of interpreting those sequences and returning them to the debugger.

Shackleford does not describe or suggest this subject matter. The Office Action relies on Figures 12 and 13 and col. 15, line 60 to col. 16, line 20. However, this alleged "processor synthesis method" does not include any mechanisms for enabling software debugging of configurable processor. The instructions referred to in cols. 15 and 16 are part of an instruction set that is built for the synthesized processor according to certain user input parameters. Nothing in Shackleford describes or suggests debugging an application on the processor by **transmitting** an instruction stream to an interpreting agent, interpreting that stream, and **returning** processor state information to the debugging application as clearly required by claims 1 and 13. Accordingly, the rejection of claims 1 and 13, as well as claims 2, 4, 8, 14, 16-18 and 20 that depend therefrom, should be withdrawn.

Amended Independent Claim 9 Patentably Defines Over Shackleford

Amended claim 9 requires is a computer readable medium including software for **generating** a configurable processor, and debugger software for generating **information necessary** to describe **save and restore instructions for state** of the configurable processor based on the user description. According to the present specification at, for example, page 13, lines 7-17, this feature allows evaluation of embedded applications on the configurable processor to occur safely and reliably.

The passage in Shackleford relied on in the Office Action (col. 21, lines 45-46) merely describes a simulation feature of the processor synthesis system (see col. 21, lines 31-33). Simulators and debuggers differ in their visibility of actual processor state and components, as well as in their overall purpose. Nothing in Shackleford describes or suggests **save and restore instructions for state** of a configurable processor, much less software for generating information necessary to describe them based on a user description of the configurable processor, as explicitly required by claim 9. Accordingly, the rejection of amended claim 9 should be withdrawn.

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[1] As set forth in the specification at page 3, lines 13-15, "debugger" refers to any software development tool that

Amended Independent Claim 10 Patentably Defines Over Shackleford

Amended independent claim 10 requires debugger software capable of **reading a description of save and restore state** information of a configurable processor and generating **saving and restoring state instruction streams** based on the description. This feature of the invention allows, for example, embedded application software to be debugged for a configurable processor, and then readily re-debugged for a changed configuration of the configurable processor.

Shackleford at col. 2, lines 9-13 merely describes an automatic module generation process (e.g. for creating layout patterns for modules). This teaches nothing about saving and restoring state of a processor, much less the software for allowing state to be saved and restored as explicitly required by claim 10. Accordingly, the rejection of this claim, along with claim 11 that depends therefrom, should be withdrawn.

Claim Rejections Under 35 U.S.C. § 103

Claims 3, 7, 12, 15 and 19 stand rejected under 35 U.S.C. § 103 as being unpatentable over Shackleford in view of U.S. Patent No. 6,142,683 to Madduri ("Madduri"). For reasons set forth more fully below, Applicants respectfully traverse this rejection.

Amended Independent Claim 12 Patentably Defines Over Shackleford and Madduri

Generally, Madduri merely teaches a solution to allow trace data to be efficiently steered between on-chip memory or off chip pins (e.g. Abstract).

Amended independent claim 12 requires, meanwhile, an instruction-insertion server that allows **retrieving** system topology information **of a chip containing multiple cores** from a computer-readable file and **determining** where elements are in a system described by the file (see the present specification at, for example, page 26, line 1 to page 31, line 3).

Nothing in Madduri or Shackleford describes or suggests the subject matter explicitly required by claim 12. Accordingly, the § 103 rejection of this claim should be withdrawn.

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requires knowledge of the state of the processor to correctly perform its function.

Claims 3, 7, 15 and 19 Patentably Define Over Shackleford and Madduri

Claims 3 and 7 depend from claim 1, which as shown above, patentably defines over Shackleford. The subject matter from claim 1 that is not taught by Shackleford is not taught by Madduri either. Accordingly, the alleged combination of Shackleford and Madduri would not have suggested the invention of claim 1, and so claims 3 and 7 are patentable at least due to their dependence from patentable claim 1.

Claims 15 and 19 depend from claim 13, which as shown above, patentably defines over Shackleford. The subject matter from claim 13 that is not taught by Shackleford is not taught by Madduri either. Accordingly, the alleged combination of Shackleford and Madduri would not have suggested the invention of claim 13, and so claims 15 and 19 are patentable at least due to their dependence from patentable claim 13.

Conclusion

All objections and rejections having been addressed, and in view of the foregoing, the claims are believed to be in form for allowance, and such action is hereby solicited. If any points remain in issue which the Examiner feels may be best resolved through a personal or telephone interview, s/he is kindly requested to contact the undersigned at the telephone number listed below.

Respectfully submitted
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